

What is claimed is:

5 1. A data processing circuit for receiving as input a plurality of packet data including packet data of at least one channel from an application side, selecting packet data of a desired channel from the input plurality of packet data, and transmitting the selected packet data to a data transmission path, comprising:

10 a channel identification data extracting circuit for extracting channel identification data regarding a selected channel in said input packet data;

15 a comparison circuit for comparing said extracted channel identification data with channel specifying data regarding a predetermined selected channel;

20 a packet data validity instruction signal generation circuit for outputting a packet data validity instruction signal indicating whether said packet data is valid or not based on said comparison result; and

a transmission circuit for selecting said input packet data to said data transmission path when said packet data validity instruction signal is valid.

25 2. A data processing circuit as set forth in claim 1, wherein said channel identification data extraction circuit receives as input a packet data input timing signal for specifying an input timing of said

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wherein said transmission circuit selects  
said input packet data and writes it to a transmission

packet data memory circuit when said packet data validity instruction signal indicates validity.

8. A data processing circuit as set forth in claim 1, wherein said transmission circuit transmits said  
5 selected packet data to said data transmission path at predetermined intervals.

9. A data processing circuit as set forth in claim 1, wherein said data transmission path is a serial bus.

Added by  
[Signature]